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Patentanmeldung Nr. Patent application No. Demande de brevet n°

02447171.6

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Application no.: 02447171.6
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INTERUNIVERSITAIR MICROELEKTRONICA CENTRUM
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BELGIQUE

Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

Photovoltaic device

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PHOTOVOLTAIC DEVICE

10 Field of the invention

[0001] The present invention is related to the field of photovoltaic devices.

State of the art

15 [0002] Within photovoltaic research, one tends to develop cost-effective solar cells, which provide a high efficiency. The costs for producing for instance silicon material based solar cells can be divided into 3 parts; the material costs, which make up the biggest part and are
20 strongly dependent on the quality of the used silicon, which is a function of its grain size, the solar cell process cost and the module process cost.

[0003] A certain type of cells, so-called HIT cell (Hetero junction with Intrinsic Thin-layer) are state of
25 the art and were developed to improve the junction properties of the classical hetero junction cell.

[0004] US patent US5,213,628 describes a photovoltaic device including a substantially intrinsic substantially amorphous semiconductor layer formed on a mono crystalline
30 or poly crystalline semiconductor layer of one conductivity type, on which a substantially amorphous semiconductor layer, being of the opposite conductivity type, is formed.

[0005] US patent US5,066,340 describes a photovoltaic device including a crystalline silicon semiconductor layer

of a first conductivity type material, an amorphous silicon semiconductor layer of the opposite conductivity type and a substantially intrinsic micro crystalline silicon semiconductor layer between these 2 layers.

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Aims of the invention

[0006] The present invention aims to describe a novel solar cell, which combines a high efficiency and a low price. The invention contributes to the continuous efforts
10 performed by industry to improve the quality of solar cells and reduce their production costs.

Summary of the invention

[0007] In a first aspect of the invention, a
15 photovoltaic device is disclosed, the device comprising a first layer based on a first semiconductor material of a first conductivity type, a second layer based on a second semiconductor material of the opposite conductivity type of the first layer, and a third layer of porous semiconductor
20 material, based on a third semiconductor material, located between the first layer and the second layer. These three layers are preferably physically attached to each other.

[0008] The first, second and third semiconductor materials can be based on the same chemical composition or
25 can be based on a different composition. Preferably the second and third semiconductor materials are based on the same chemical composition. Most preferably the second and third semiconductor material are based on silicon.

[0009] In a first embodiment of the first aspect of the
30 present invention, the third semiconductor material is based on substantially non-doped semiconductor material.

[0010] In a further embodiment of the first aspect and possibly combined with the first embodiment of the first aspect of the present invention, the third semiconductor

material is based on crystalline semiconductor material, preferably mono crystalline or multi crystalline.

[0011] According to a further embodiment of the first aspect of the present invention and possibly combined with
5 any of the previously mentioned embodiments, the first semiconductor material is based on substantially amorphous semiconductor material, substantially nano crystalline semiconductor material or substantially microcrystalline semiconductor material.

10 [0012] According to a further embodiment of the first aspect of the present invention and possibly combined with any of the previously mentioned embodiments, the second semiconductor material is based on crystalline semiconductor material, with specific embodiments of having
15 the second semiconductor material based on mono crystalline or multi crystalline semiconductor material.

[0013] According to a further embodiment of the first aspect of the present invention and possibly combined with any of the previously mentioned embodiments, the first
20 layer has a thickness between 3nm and 100nm.

[0014] According to a further embodiment of the first aspect of the present invention and possibly combined with any of the previously mentioned embodiments, the third layer has a thickness between 1nm and 50nm.

25 [0015] A first method is disclosed for producing a photovoltaic device comprising the steps of providing the second layer, depositing the third layer on the second layer and depositing the first layer on the third layer, whereby the layers are as described before.

30 [0016] In a second aspect of the present invention, a photovoltaic device is disclosed, whereby the second layer of is further attached to a fourth layer which is porous and based on substantially non-doped crystalline semiconductor material, which is on its turn attached to an

fifth layer based on amorphous, nano crystalline or microcrystalline silicon semiconductor material and of the same conductivity type as the second layer.

[0017] A second method is disclosed which is based on the first method, further comprising the steps of depositing the fourth layer on the second layer and depositing the fifth layer on the fourth layer.

SHORT DESCRIPTION OF FIGURES

10 [0018] Fig. 1 shows a schematic representation of an aspect of the invention.

[0019] Fig. 2 shows a schematic representation of another aspect of the invention.

[0020] Fig. 3 shows the relation between the short circuit current [mA/cm^2] and the thickness of porous layer is depicted.

[0021] Fig. 4 illustrates the relation between open circuit voltage [mV] versus thickness of porous layer.

[0022] Fig. 5 shows the relation between efficiency [%] and thickness of porous layer is represented.

[0023] Fig. 6 shows the fill factor [%] values for different values of porous layer thickness.

Detailed description of the invention

25 [0024] The following description and examples illustrate preferred embodiments of the present invention in detail. Those of skill in the art will recognize that there are numerous variations and modifications of this invention that are encompassed by its scope. Accordingly, the description of preferred embodiments should not be deemed to limit the scope of the present invention.

[0025] For the purpose of this invention, the naming of crystals is based on their grain sizes, and is represented

in Tab. 1. The term "crystalline silicon" refers to silicon of all crystal types except amorphous silicon.

<u>Grain size of silicon crystal</u>	<u>Name</u>
Substantially Atomic size	Amorphous
<10 nm	Nano crystalline
<1 μm	Micro crystalline
<100 μm	Poly crystalline
<1 mm	Multi crystalline
Infinite	Mono crystalline

Tab. 1 : naming of crystals based on their grain sizes

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[0026] For the purpose of this invention, semiconductor material can be, but is not limited to, Si: Silicon, Ge: Germanium, GaP: Gallium Phosphide, GaAs: Gallium Arsenide, InAs: Indium Arsenide, C: Diamond, GaSb: Gallium Antimonide, InSb: Indium Antimonide, InP: Indium Phosphide, GaAs_{1-x}Sb_x: Gallium Arsenide Antimonide, Al_xGa_{1-x}As: Aluminium Gallium Arsenide, Ga_xIn_{1-x}P: Gallium Indium Phosphide, Ga_xIn_{1-x}As: Gallium Indium Arsenide, Ga_xIn_{1-x}Sb: Gallium Indium Antimonide, InAs_{1-x}Sb_x: Indium Arsenide Antimonide, Ga_xIn_{1-x}As_yP_{1-y}: Gallium Indium Arsenide Phosphide, Ga_xIn_{1-x}As_ySb_{1-y}: Gallium Indium Arsenide Antimonide, GaN: Gallium Nitride, AlN: Aluminium Nitride, InN: Indium Nitride, whereby x and y are natural numbers. Preferably semiconductor material refers to Si, Ge, GaAs.

20 Most preferably it is Silicon.

[0027] For the purpose of this invention the wording '...semiconductor material ... based on...' is used to indicate the possibilities of: (a) having impurities (called dopants

in the art) typically introduced in the semiconductor material during doping procedures. (b) having impurities in the semiconductor material that do not bring significant changes in the conductivity properties of the semiconductor material.

[0028] In a first aspect of the invention, a photovoltaic device is disclosed (Fig. 1A), comprising a first layer of a first semiconductor material of a first conductivity type (1), a second layer of a second semiconductor material of the opposite conductivity type (2) of the first layer, and a third layer made of porous semiconductor material (3) of a third semiconductor material, located between the first layer and the second layer. These three layers are preferably physically attached to each other. The first, second and third semiconductor materials can be based on the same chemical composition or can be based on a different composition. Preferably the second and third semiconductor materials are based on the same chemical composition. Most preferably the second and third semiconductor material are based on silicon.

[0029] In a typical production process the porous third layer can be created by elaboration of the second layer. The second layer can be, but is not limited to, a wafer or processed wafer. The first layer (called emitter layer in the art) can typically be covered with a conductive electrode layer (5), which can be substantially transparent and can be used for the transport of photon-generated electrons towards the front contacts (6). The conductive electrode layer can be made of for instance Indium Tin Oxide (ITO), SnO_2 or ZnO . On the backside of the second layer (called bulk layer in the art) a back electrode is provided (4), which can be substantially consisting of a

metal as for instance, but not limited to, Aluminum, Silver, Nickel. The backside of the bulk layer is defined as the one of the substantially 2 surfaces of the bulk layer, which is the most distant from the third layer.

5 [0030] Porous semiconductor material is state-of-the-art. It is a medium substantially consisting of semiconductor material and voids, where the percentage of the total volume occupied by voids can be typically between 10% and 85%. The terms n-type conductivity and p-type
10 conductivity are known to a person ordinary skilled in the art.

[0031] In a further embodiment of the first aspect of the present invention the third layer can be made of porous substantially non-doped semiconductor material. Non-doped
15 semiconductor material is semiconductor material, which has not explicitly been doped or has no characteristics similar to such material and is also referred to in the art as 'intrinsic semiconductor material'.

[0032] In another embodiment of the first aspect of the
20 present invention the third layer is made of porous substantially non-doped semiconductor material, which is based on crystalline semiconductor material. In another embodiment of the first aspect of the present invention the third layer is made of porous substantially non-doped
25 silicon semiconductor material, based on crystalline semiconductor material, with specific embodiments of having the third layer made from mono crystalline silicon semiconductor material or multi crystalline silicon semiconductor material.

30 [0033] According to a further embodiment of the first aspect of the present invention and possibly combined with any of the previously mentioned embodiments, the first layer is based on substantially amorphous semiconductor material, substantially nano crystalline semiconductor

material or substantially microcrystalline semiconductor material.

[0034] According to a further embodiment of the first aspect of the present invention and possibly combined with any of the previously mentioned embodiments, the second layer is based on crystalline semiconductor material, with specific embodiments of having the second layer based on mono crystalline or multi crystalline silicon semiconductor material.

10 [0035] In a further embodiment of the first aspect of the present invention; the second layer consists substantially of multi crystalline silicon semiconductor material of p-type conductivity, the first layer is made of amorphous silicon semiconductor material of n-type conductivity, and the third layer is made of porous non-doped silicon semiconductor material based on multi crystalline semiconductor material between the first layer and the second layer.

[0036] The thickness of the first layer is preferably within the range of [3nm, 100nm]. The thickness of the third layer is preferably within the range of [1nm, 50nm]. The second layer has a typical appropriate bulk layer thickness.

[0037] Fig. 3, Fig. 4, Fig. 5 and Fig. 6 are representing measurements of typical solar cell parameters as there are respectively the short circuit current $J_{sc}[mA/cm^2]$, the open circuit voltage $V_{oc}[mV]$, efficiency $\eta[\%]$ and fill factor $FF[\%]$, based on typical but specific layer thicknesses for the emitter layer and the bulk layer, this for a reference, further mentioned below, and for different thicknesses of the porous layer: 16nm, 24nm, 36nm.

[0038] A preferred embodiment consists of a multi crystalline Silicon substrate (Baysix, carrier concentration of about $10^{16}cm^{-3}$), on which a porous layer is electrochemically elaborated, having a thickness with a value between 15nm - 20nm and a porosity of about 20%. The remaining non-porous part of the wafer is p-doped. A PECVD process is used to deposit an amorphous silicon layer on top with a thickness of about 10-15 nm, which has been hydrogenated and n-doped. (carrier concentration of about $10^{19}cm^{-3}$).

[0039] The results indicate an optimal porous layer thickness to be preferably around 16nm, while for larger and smaller values the efficiency decreases, and indicate that the concept works for a thickness of the porous layer within the range of [1nm, 50nm] for typical emitter thickness, which is preferably within the range of [3nm, 100nm].

[0040] The efficiency is higher then in an prior art reference device where substantially non-doped amorphous silicon was used for the third layer, as illustrated in Tab. 2.

[0041] The reference device consists of a p-doped multi crystalline Silicon wafer (Baysix, carrier concentration of about $10^{16}cm^{-3}$), on which a 5nm thick layer of intrinsic amorphous silicon is deposited via a PECVD technique. Another PECVD process is used to deposit an amorphous silicon layer on top with a thickness of about 10-15 nm, which has been hydrogenated and n-doped (carrier concentration of about $10^{19}cm^{-3}$).

	$V_{oc}[mV]$	$J_{sc}[mA/cm^2]$	$FF[\%]$	$\eta[\%]$
Invention	579	32.63	75	14.2
Amorphous non-doped silicon as thin film layer	572.0	30.08	76.6	13.2

Tab. 2: comparison of characteristic parameters between the invention and an equivalent study with a substantially non-doped amorphous third layer.

5 [0042] A first characteristic of the invention is that substantially non-doped porous silicon based on crystalline silicon has electrical characteristics (carrier concentration is in the region of $10^{12}cm^{-3}$ – $10^{13}cm^{-3}$) similar to those of substantially non-doped amorphous silicon
10 (carrier concentration is in the region of $10^{11}cm^{-3}$), more precisely it is not conductive, but it has lower absorption characteristics than amorphous silicon. Non-doped amorphous silicon absorbs substantially more light. This implies that the present invention can have a thicker third layer (in
15 the art called 'thin film layer'), improving robustness against diffusion of Indium atoms coming from the ITO towards the bulk material.

[0043] Moreover porous silicon is intrinsically hydrogen (H) rich, increasing passivation. Since grain boundaries
20 between neighboring single crystals in a multi crystalline layer also increase recombination activity of the cell, it needs to be passivated. In the presence of Aluminum (Al), typically used as electrode material, H atoms coming from the porous silicon are diffusing quicker through the multi
25 crystalline silicon and an improved passivation of the bulk material is achieved ['Synergetic effect of Aluminum and thermally treated porous silicon for bulk passivation of

multi crystalline silicon', R. Bilyalov, Z. Matic, J. Poortmans, F. Schomann, W. Schmidt, Conference Record of the Twenty-Eighth IEEE Photovoltaic Specialists Conference - 2000 (Cat. No.00CH37036). IEEE, Piscataway, NJ, USA; 5 2000; xxxii+1838 pp. p.291-4].

[0044] Porous silicon can be achieved by electrochemical etching or chemical etching.

[0045] A second characteristic of the invention is that after the production of the porous layer by elaboration of 10 the second layer, no extra plasma-cleaning step can be required before adding the amorphous emitter layer on top, which would be needed in case of a substantially non-doped amorphous silicon thin film as third layer.

[0046] Moreover in the latter case a wet cleaning step 15 is required before the PECVD process that deposits for instance the substantially non-doped amorphous silicon thin film, which implies that the deposition of electrode material on the backside, typically Aluminum, can only be performed after the wet cleaning process, polluting the 20 front surface. In the case of a substantially non-doped porous thin film, where the porous layer is made through electrochemical etching this contamination will be removed during the production process.

[0047] In the case of a porous layer formed by chemical 25 etching, the production of the device represented in Fig. 2, where the multi crystalline or mono crystalline bulk layer has to be on both sides covered with porous silicon material, can be simplified, since both layers can be formed simultaneously.

30 [0048] The invention also relates to a photovoltaic device (Fig. 2B), whereby the second layer of (Fig. 1A) is further attached to a fourth layer (7) made of porous substantially non-doped silicon semiconductor material, based on crystalline semiconductor material, which is on

its turn attached to a fifth layer (8) based on amorphous silicon semiconductor material and of the same conductivity type as the second layer, similar to the photovoltaic cell construction as in [Toru Sawada, Norihiro Terada, Sadaji
5 Tsuge, Toshiaki Baba, Tsuyoshi Takahama, Kenichiro Wakisaka, Shinya Tsuda and Shoichi Nakano, High-efficiency a-Si/c-Si hetero junction solar cell, First WCPEC , Hawaii, 1994, pp. 1219-1226].

CLAIMS

1. A photovoltaic device, comprising a first layer of a first semiconductor material of a first conductivity type, a second layer of a second semiconductor material of the opposite conductivity type of said first layer, and a third layer of a third semiconductor material wherein:

- said third layer is located between said first layer and said second layer; and
- said third layer is porous.

2. The photovoltaic device according to claim 1, wherein the first semiconductor material, the second semiconductor material and the third semiconductor material are based on the same chemical element or chemical element combination.

3. The photovoltaic device according to claim 1, wherein the second semiconductor material and the third semiconductor material are based on the same chemical element or chemical element combination.

4. The photovoltaic device according to claim 3, wherein the chemical element is silicon.

5. The photovoltaic device according to claim 1 to 4, wherein the third semiconductor material is non-doped.

6. The photovoltaic device according to claim 1 to 5, wherein the third semiconductor material is crystalline.

7. The photovoltaic device according to claim 1 to 6, wherein said third layer is based on material selected from the group consisting of multi crystalline semiconductor material and mono crystalline semiconductor material.

8. The photovoltaic device according to claim 1 to 7, wherein the second layer is based on crystalline semiconductor material.

5 9. The photovoltaic device according to claim 8, wherein the second layer is based on material selected from the group consisting of mono crystalline semiconductor material and multi crystalline semiconductor material.

10 10. The photovoltaic device according to claim 1 to 9, wherein the said first layer has a thickness between 3nm and 100nm.

11. The photovoltaic device according to claim 1 to 10, wherein the third layer has a thickness between 1nm and 50nm.

15 12. A method for providing a photovoltaic device comprising the steps of:

- providing the second layer described in any of the previous claims; and
- depositing the third layer described in any of the previous claims on said second layer; and
- 20 - depositing the first layer described in any of the previous claims on said third layer.

13. A photovoltaic device according to claim 1 to 11, whereby the second layer is further attached to a fourth layer which is porous and based on a fourth semiconductor material, said fourth semiconductor material being non-doped crystalline silicon semiconductor material, and said fourth layer being attached to a fifth layer based on material selected from the group consisting of amorphous silicon semiconductor material, nano crystalline semiconductor material and micro crystalline silicon semiconductor material, said fifth layer being of the same conductivity type as the said second layer.

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14. A method according to claim 12 further comprising the steps of:

- depositing the fourth layer described in claim 13 on said second layer; and
- 5 - depositing the fifth layer described in claim 13 on said fourth layer.

ABSTRACTPHOTOVOLTAIC DEVICE

5 The present invention is related to a
photovoltaic device, comprising a first layer of a first
semiconductor material of a first conductivity type, a
second layer of a second semiconductor material of the
opposite conductivity type of the first layer, and a third
10 layer of a third semiconductor material located between the
first layer and the second layer which is porous. The
present invention also provides a method for producing the
photovoltaic device.

15

(Figure 1)

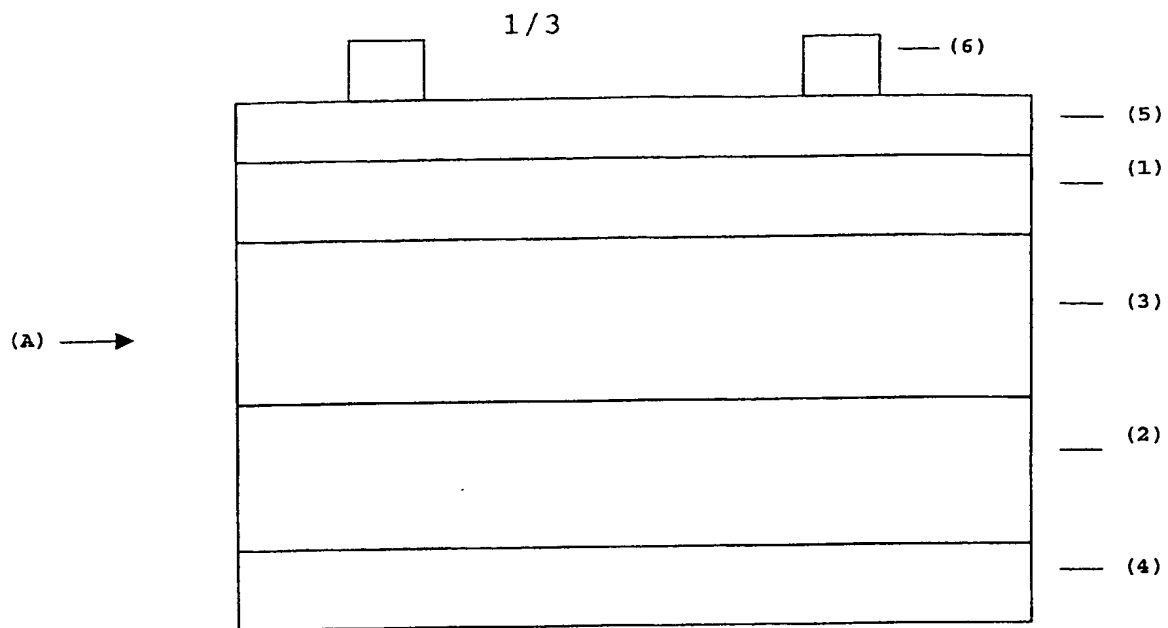


Fig. 1

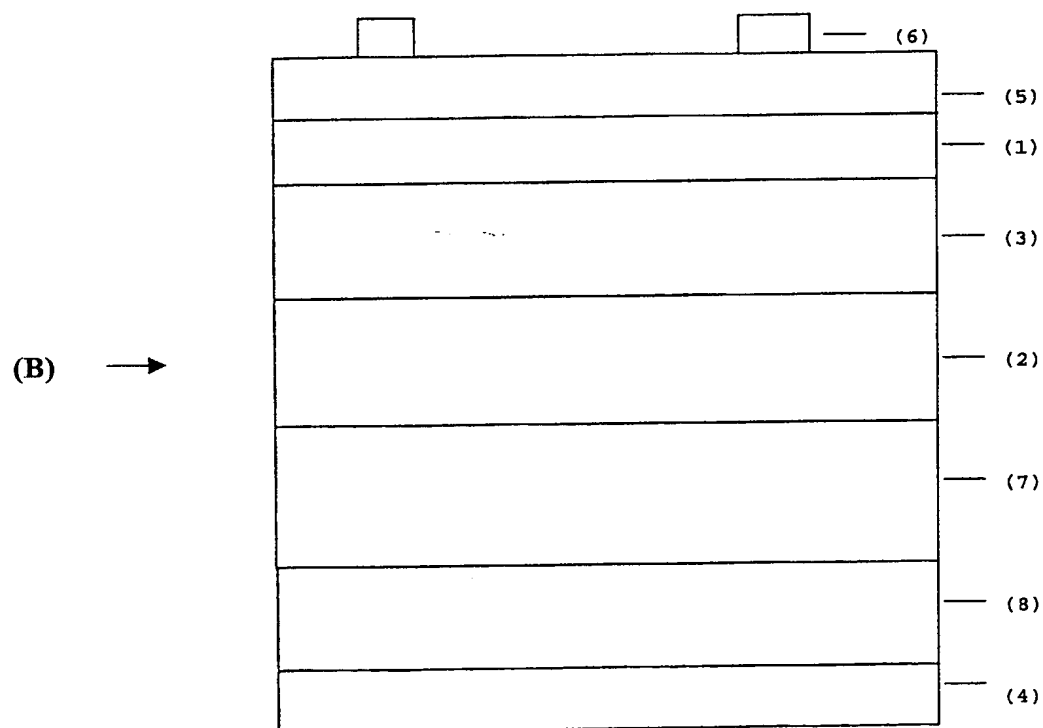
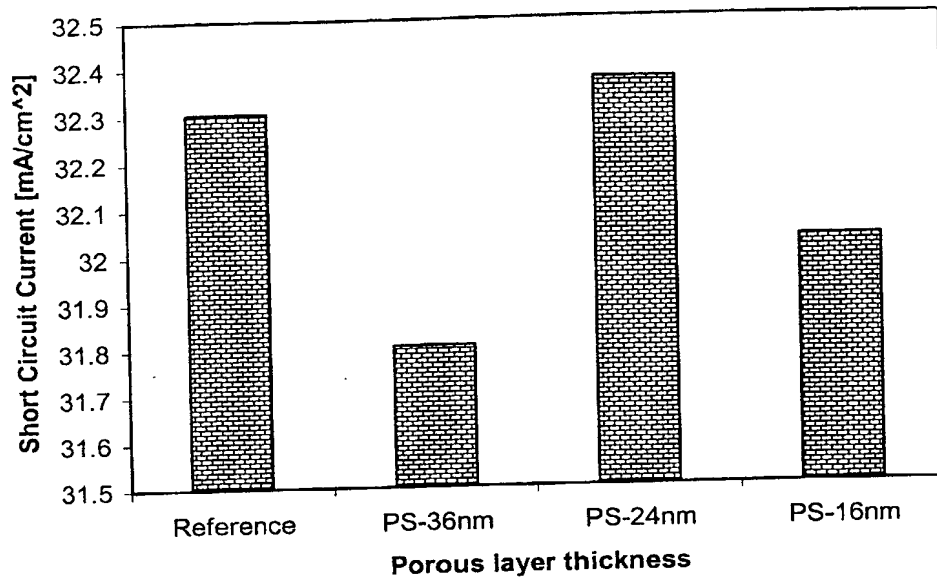
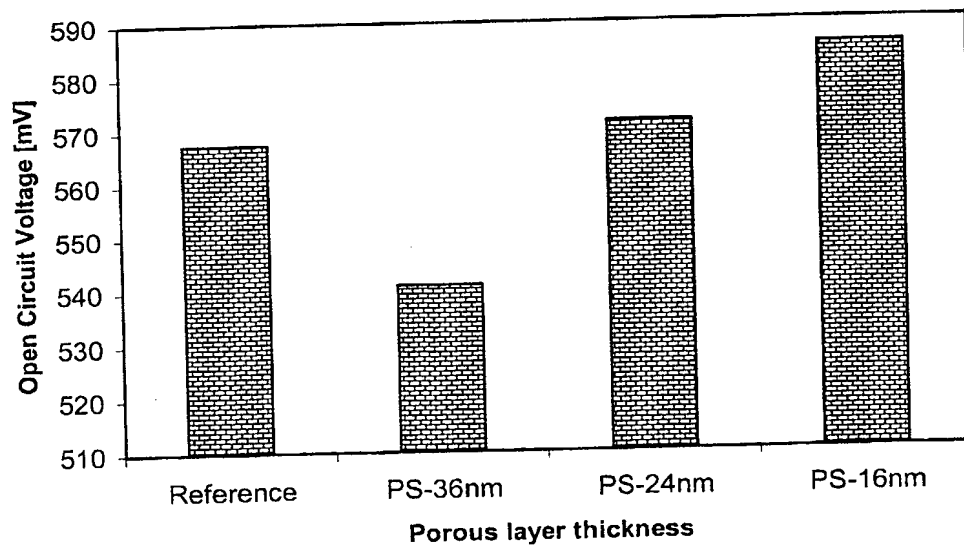
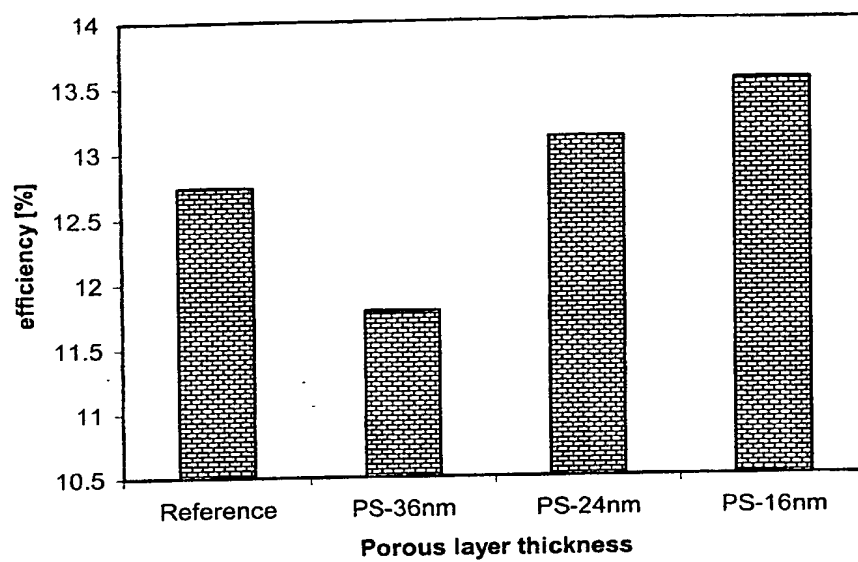
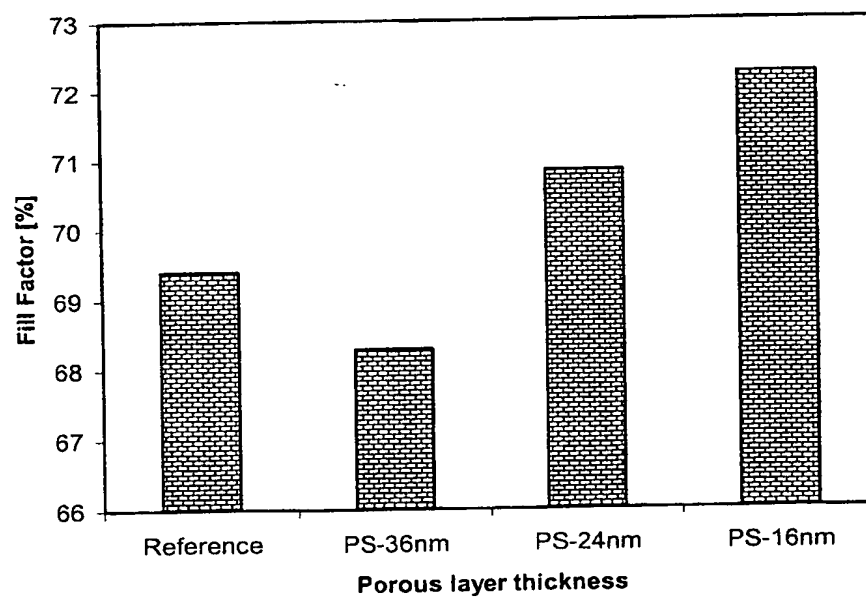


Fig. 2

Fig. 3Fig. 4

Fig. 5Fig. 6

